REMARKS

Claims 1-15 are pending. Claim 4 has been amended. No new matter has been added.

Disclaimers Relating to Claim Interpretation and Prosecution History Estoppel

Claim 4 has been amended notwithstanding the belief that this claim was allowable. Except as specifically admitted below, no claim elements have been narrowed. Rather, cosmetic amendments have been made to the claims and to broaden them in view of the cited art. The amendments to claims 4 were not necessary for patentability.

Any reference herein to "the invention" is intended to refer to the specific claim or claims being addressed herein. The claims of this Application are intended to stand on their own and are not to be read in light of the prosecution history of any related or unrelated patent or patent application. Furthermore, no arguments in any prosecution history relate to any claim in this Application, except for arguments specifically directed to the claim.

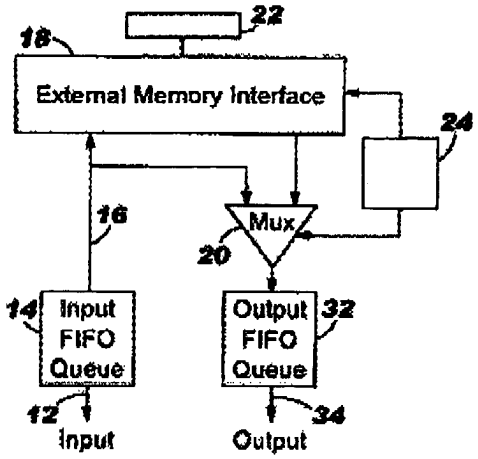
Claim Objections

The Examiner objected to claim 4 due to an informality. The Examiner suggested that in claim 4, line 2, "number of blocks of having the selected block size" should be -- number of blocks of **data** having the selected block size--. This amendment has been made so withdrawal of the objected is merited.

Claim Rejections - 35 USC § 103

The Examiner rejected claims 1-15 under 35 USC § 103(a) as obvious from Bass et al (USP 6,557,053) in view of Shimizu (USP 5,905,911). This rejection is respectfully traversed.

Bass is directed to a queue manager for a buffer. Bass discloses an input FIFO 14,[1] an output FIFO 32, an external memory 22, a multiplexer 20 and control logic 24:



In Bass, data leaving the input FIFO 14 goes to both the external memory 22 and the mux 20. Furthermore the mux can select data from either the memory 22 or the input FIFO 14. This is controlled by the control logic 24. The input FIFO and output FIFO are smaller and faster than the external memory. Bass discloses and teaches that the control logic 24 is used to maximize utilization of the input FIFO and the output FIFO. The control logic 24 directs data into the output FIFO so long as the input FIFO and output FIFO "are full or at least have a predetermined percentage capacity full."[2] "Thus, as long as the amount of input data 12 being read from an external source does not exceed a preselected capacity of the input FIFO buffer 14 and output FIFO buffer 32, the data is passed from the input FIFO buffer 14 directly to the output FIFO buffer32."[3]

Bass suggests that the designer could select the block size and the number of blocks in a memory transfer burst. However, Bass does not disclose, teach or suggest that this could be done dynamically, and certainly does not disclose, teach or suggest that the control logic could or should

[1] The arrow on the data input 12 appears to be pointing the wrong way.
[2] Bass 2:21-24.
[3] Bass 2:32-36.

perform such a function. In Bass, it appears that both the block size and the number of blocks are preset.

Shimizu is directed to a data transfer system which determines a size of data being transferred between a memory and an I/O device. Shimizu in relevant part states, "a data transfer size is determined automatically to maximize the transfer efficiency in accordance with an amount of data stored in the buffer of, for example, the input device and a check on memory address alignment." Column 4, lines 63-67. In Shimizu, the primary goal is to achieve memory address alignment, and the secondary goal is to transfer as much data as possible at one time while still achieving memory address alignment.

To achieve its goals, Shimizu discloses a system wherein an input device 13 has an input FIFO 12 and an output device 17 has an output FIFO 16. *See* FIG. 4. A memory write controller (i.e., a direct memory access controller, DMAC) 14 controls data transfers from the input FIFO 12 to the memory 9. *See* FIG. 4(a). A memory read controller 18 (which apparently is also the DMAC) controls data transfers from the memory 10 to the output FIFO 16. *See* FIG. 4(b). Shimizu discloses that the input FIFO 12 and the output FIFO 16 store data as blocks, and the blocks contain a variable number of words. The words appear to have a fixed length. In Shimizu data is not transferred between the FIFOs and the memory in units of blocks. Instead, the DMAC causes a variable number of words to be transferred between the FIFOs and the memory. In Shimizu, it appears that the block size is always fixed, and Shimizu nowhere appears to disclose, teach or suggest transferring more than one block between a FIFO and memory.

The invention of claim 1 is a caching system which includes a tail FIFO, a memory, a head FIFO, a multiplexer and a controller. The controller is "operable to transfer a dynamically selected number of blocks of data from the incoming frames having a dynamically selected block size from the tail FIFO to the memory and from the memory to the head FIFO, wherein the selected block size and the selected number of blocks together provide maximum memory transfer efficiency level." Neither Bass nor Shimizu has any disclosure, teaching or suggestion of caching system having a

controller as claimed. The references, neither alone nor together, disclose, teach or suggest "a dynamically selected number of blocks" or "a dynamically selected block size". Thus, claim 1 is not obvious from Bass in view of Shimizu.

The invention of claim 10 is a method for implementing a caching system. Claim 10 recites the step of "dynamically determining a block size and number of blocks to support the maximum efficiency level." As explained, Bass and Shimizu have no disclosure, teaching or suggestion of such a step. Thus, claim 10 is not obvious from Bass in view of Shimizu.

The invention of claim 12 is a caching system. The controller is "operable to transfer a dynamically selected number of blocks of data from the incoming frames having a dynamically selected block size from the tail FIFO to the memory and from the memory to the head FIFO, wherein the selected block size and the selected number of blocks together provide maximum memory transfer efficiency level." Bass and Shimizu have no disclosure, teaching or suggestion of a caching system having a controller as claimed. Thus, claim 12 is not obvious from Bass in view of Shimizu.

In sum, the rejection of claims 1-15 as obvious from Bass in view of Shimizu should be withdrawn.

Conclusion

It is submitted, however, that the independent and dependant claims include other significant and substantial recitations which are not disclosed in the cited references. Thus, the claims are also patentable for additional reasons. Also, the Examiner proposed a combination of Shimizu and Bass; however, it is clear that such a combination would be inoperable. For economy these additional grounds for patentability are not set forth here in detail.

In view of all of the above, it is respectfully submitted that the present application is now in condition for allowance. Reconsideration and reexamination are respectfully requested and allowance at an early date is solicited.

The Examiner is invited to call the undersigned attorney to answer any questions or to discuss steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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